TITLE OF THE INVENTION

METHOD AND APPARATUS FOR CONTROLLING POWER SUPPLIED TO LASER DIODE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of Korean Application No. 99-18848, filed May 25, 1999, in the Korean Patent Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method and apparatus for controlling power supplied to a laser diode to an optimal level in an optical recording/playback apparatus, and more particularly, to a method and apparatus for controlling the power supplied to the laser diode, so that fluctuation in the power of the laser diode, which occurs at a record/playback area of an optical disc, can be prevented.

2. Description of the Related Art

With the advent of multimedia, the demand for high-density recording media has increased. Such high-capacity recording media include magnetic optical disc drives (MODD), digital versatile disc-read only memory (DVD- ROM) drives, DVD-random access memory (DVD- RAM) drives and the like.

Such optical recording apparatuses must be optimized with high-accuracy depending on the type of optical recording medium used. In order to ensure accurate recording/playback of data, such optical recording apparatuses include an automatic laser diode power control (APC) circuit for controlling the power applied to a laser diode (LD).

FIG. 1 is a block diagram showing the structure of an APC circuit in a conventional optical recording apparatus. In FIG. 1, reference numeral 120 represents a write waveform generator for generating write pulses to form spaces and marks according to data to be

recorded, reference numeral 140 represents an LD driver for controlling the power of an LD 160 according to the write pulses generated by the write waveform generator 120. Data to be recorded is input to the write waveform generator 120, in the form of a non return to zero inverted (NRZI) signal. Also, in the case of a DVD-RAM, a combination of a first pulse, a last pulse, a cooling pulse and a multi-pulse train is output.

An APC circuit 200 includes a photo diode (PD) 202, a variable gain amplifier (VGA) 204, a comparator (COMP) 206, an up/down counter 208 and a digital-to-analog converter (DAC) 210. The PD 202 receives laser beams reflected by a disc 180, and generates a current signal corresponding to the amount of the received laser beam. The VGA 204 amplifies the current signal from the PD 202 to a predetermined gain and converts the current signal into a voltage signal. The COMP 206 compares the output from the VGA 204 to a reference voltage Vref, and outputs a binary decision signal indicating which one is higher than the other, according to the comparison result.

The up/down counter 208 performs up or down counting based on the comparison result from the COMP 206. If the decision signal from the COMP 206 represents that the output from the VGA 204 is higher than the reference voltage Vref, for example, if the decision signal is low, the up/down counter 208 performs up-counting. Meanwhile, if the decision signal represents that the output from the VGA 204 is lower than the reference voltage Vref, for example, if the decision signal is high, the up/down counter 208 performs down-counting. The count result from the up/down counter 208 is applied through the DAC 210 to the LD driver 140. The LD driver 140 controls the amount of power supplied to the LD 160 according to the amplitude of the signal applied from the DAC 210.

The APC circuit 200 of FIG. 1 detects the difference between the output level of the LD 160, which is detected by the PD 202, and the reference voltage, and controls the power supplied to LD 160 in accordance with the detected difference. However, in the APC circuit 200 of FIG. 1, the output from the LD 160 continuously changes even at an effective data area of the disc 180 due to a continuous operating characteristic of the up/down counter 208. Thus, it is difficult to obtain an accurate recording/playback result. In addition, the APC 200 is susceptible to external noise.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an improved method of controlling the power supplied to a laser diode (LD) even at an effective data area of a disc.

Another object of the present invention is to provide an apparatus for controlling the power of an LD by this method.

Additional objects and advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

According to an aspect of the present invention, there is provided a method of controlling the power of a laser diode by using a difference between the laser level reflected by a disc and a reference level, the difference being detected after the laser level reflected by the disc is compared with the reference level, the method comprising: (a) generating a periodic synchronization signal; and (b) controlling the power of the laser diode in synchronism with the synchronization signal.

According to another aspect of the present invention, there is provided an apparatus for controlling the power of a laser diode, comprising: a photo diode which receives a laser reflected by a disc to generate a current signal corresponding to the level of the received laser; a comparator which comprises the output from the photo diode with a reference voltage and outputs a binary decision signal which indicates which input for the comparison is higher than the other input; an up/down counter which up/down counts the binary decision signal in accordance with the comparison result of the comparator; a laser diode driver which controls the power level of the laser diode according to the count result of the up/down counter; and a controller which controls the automatic power control of the laser diode (APC controller), interposed between the up/down counter and the laser diode driver, the APC controller latching the output of the up/down counter in synchronism with a periodic synchronization signal, and outputting the latch result to the laser diode driver.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a block diagram showing the structure of a conventional automatic laser diode power control (APC) circuit;

FIG. 2 is a block diagram showing a structure of an apparatus for controlling the power supplied to a laser diode (LD) according to an embodiment of the present invention;

FIGS. 3A through 3D illustrate a relationship between a sector format of a digital versatile disc-random access memory (DVD-RAM) and mirror and gap signals;

FIGS. 4A through 4E show waveforms illustrating the operation of the apparatus shown in FIG. 2; and

FIG. 5 is a block diagram showing a detailed structure of the apparatus of FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now made in detail to the present preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

Referring to FIG. 2, which is a block diagram showing the structure of an apparatus for controlling the power supplied to a laser diode (hereinafter, referred to as automatic laser diode power control (APC) circuit), elements that perform the same as those of FIG. 1 are represented by the same reference numerals as those used in FIG. 1, and an explanation thereof will be omitted. Reference numeral 300 represents an APC controller and reference numeral 310 represents a control signal generator.

The APC controller 300 controls the output from the digital-to-analog converter (DAC) 210 according to the selected APC mode. In the present invention, the APC mode includes a sub-APC mode, an average APC mode and a sub-average APC mode. The sub-APC mode refers to a mode where the APC is controlled at a non-data recording area of a disk and the

control value is maintained up to the following area of the disc. In a digital versatile disc-random access memory (DVD-RAM), the non-data record area includes, for example, a mirror or gap area.

In the average APC mode, the average of the current control value from the DAC 210 and a previous control value obtained prior to a predetermined time through APC control performed preceding the current APC control is provided to the laser diode (LD) driver 140. Also, in the sub-average APC mode, an average of control values from the non-data recording area of the disc, such as mirror or gap area is obtained, and the average is maintained up to the following area of the disc.

The control signal generator 310, which is controlled by a microcomputer (not shown), controls an operating mode and operating area of the APC controller 300 while a mirror or gap signal MIRROR/GAP is applied.

FIGS. 3A through 3D illustrate the relationship between the format of a sector of a DVD-RAM, and mirror and gap signals. As shown in FIGS 3A through 3B, the sector of the DVD-RAM essentially includes a header area, a mirror area 402 and a data recording area. A header signal for tracking control is recorded in the header area, and no signal is recorded in the mirror area 402 according to specifications. In the data recording area which includes a gap area 404, a sector address, data and the like are recorded. As shown in FIG. 3C, a mirror signal MIRROR indicates the mirror area 402 of the disk and, as shown in FIG. 3D, a gap signal GAP indicates the gap area 404 of the disk.

FIGS 4A through 4E show waveforms illustrating the operation of the APC circuit shown in FIG. 2. FIG 4A shows a waveform of a mirror or gap signal MIRROR/GAP, FIG. 4B represents laser power fluctuation in the conventional APC circuit shown in FIG. 1, in which APC is performed over the entire area of the disc. Also, FIG. 4C through 4E illustrate laser power fluctuation in the sub-APC mode, the average APC mode and the sub-average APC mode, respectively, in the APC circuit shown in FIG. 2.

As shown in the waveform of FIG. 4C, in the sub-APC mode, a control value, which is latched at the end of the mirror or gap area, is maintained up to the following mirror or gap area. Also, in the average APC mode, shown in the waveform of FIG 4D, the average of

control values is used, so that the laser power does not sharply change within an APC range. In the sub-average APC mode shown in the waveform of FIG. 4E, the average of control values in the mirror or gap area is maintained up to the next mirror or gap area.

In the sub-APC mode or sub-average APC mode, the APC circuit of FIG. 2 performs APC over a period of one sector because the mirror and gap signals MIRROR/GAP are generated once every sector. Also, since the APC is performed in a non-data recording area such as a mirror area, or in an area that is not used, such as a gap area, continuous fluctuation in laser power does not occur.

In the average APC mode, the APC circuit shown in FIG. 2 shows resilience against external noise, by using the average of the current and preceding control values. That is, the average APC mode provides an effect of low-pass-filtering the control values, so that the APC operation in the average APC mode is resilient against external noise that may contain a radio frequency (RF) component.

FIG. 5 is a block diagram showing a detailed structure of the APC circuit of FIG. 2. In FIG. 5, elements which perform in the same manner as those of FIG. 1 are represented by the same reference numerals as those used in FIG. 1. The gain of the VGA 204 is varied according to control signals WR and ER, which are applied thereto. The comparator (COMP) 206 includes a first COMP 206a which is used in a playback mode, and a second COMP 206b which is used in erase and record modes. The up/down counter 208 includes five counters 208a through 208e. The first up/down counter 208a is used in a read mode, the second up/down counter 208b is used for lands in the erase mode, the third up/down counter 208c is used for grooves in the erase mode, the fourth up/down counter 208d is used for lands in the erase and record modes, and the fifth up/down counter 208e is used for grooves in the erase and record modes.

The DAC 210 includes three DACs 210a through 210c. The first DAC 210a is used in the read mode, the second DAC 210b is used in the erase mode, and the third DAC 210c is used in the record mode. Also, a MUX 212 including first and second MUXs 212a and 212b couples the second through fifth counters 208b through 208e, to the second and third DACs 210b and 210c, according to whether the current mode is the erase or record mode and

whether the current track is a land or groove. The first MUX 212a is used to couple the second and third counters 208b and 208c to the second DAC 210b in the erase mode, and the second MUX 212b is used to couple the fourth and fifth counters 208d and 208e to the third DAC in the record mode.

A BUF 214 including first through third BUFs 214a through 214c buffers the outputs from the first through third DACs 210a through 210c and provides the buffered results to the LD driver 140. In the read mode, the first BUF 214a buffers the output from the first DAC 210a and outputs the result to the LD driver 140, the second BUF 214b buffers the output from the second DAC 210b and outputs the result to the LD driver 140, and the third BUF 214c buffers the output from the third DAC 210c and outputs the result to the LD driver 140.

First and second reference voltages Vref1 and Vref2 are provided to the COMP 206 by the operation of latches 216 and 217, fourth and fifth DACs 218 and 219, fourth and fifth BUFs 220 and 221, and a third MUX 222. The latch 216, which is for use in a read mode, latches a reference data RD1 which is provided from the microcomputer in the read mode, and provides the latched data to the fourth DAC 218. The fourth DAC 218 converts the latched data into analog data, and the fourth BUF 220 outputs the analog data from the fourth DAC 218, as the first reference voltage Vref1 for the read mode, to the first COMP 206a. The latch 217, which is for use in erase and record modes, latches reference data RD2_1, RD2_2, RD2_3 and RD2_4 which are provided from the microcomputer in the erase and record modes. The latch 217 includes first through fourth latches 217a through 217d. The first latch 217a latches the reference data RD2_1 for the erase mode and lands, the second latch 217b latches the reference data RD2_2 for the erase mode and grooves, the third latch 217c latches the reference data RD2_3 for the record mode and lands, and the fourth latch 217d latches the reference data RD2_4 for the record mode and grooves.

The third MUX 222 selectively outputs one of the outputs from the first through fourth latches 217a through 217d according to whether the current mode is the erase or record mode and whether the current track is a land or groove. The fifth DAC 219 converts the data from the third MUX 222 into analog data, and the fifth BUF 221 outputs the analog data from the fifth DAC 219, as the second reference voltage Vref2 for the erase and record modes, to the

second COMP 206b. Here, the number of up/down counters, DACs and COMPs may be varied.

The APC controller 300 controls the value to be provided to the DAC 210 in accordance with the APC mode selected by the microcomputer. The control signal generator 310, which is controlled by the microcomputer, controls the operating mode and operating area of the APC controller 300 while the mirror or gap signal MIRROR/GAP is applied. A divider 320 divides a reference clock signal CK of a drive to generate a periodic signal DV. In a disc such as a DVD-RAM, which has no mirror or gap area, the control signal generator 310 controls the operating mode and operating area of the APC controller 300 according to the periodic signal, which is division signal DV, from the divider 320. In such cases, the APC operation is periodically performed. Also, the period of the APC operation can be controlled by varying a division ratio in the divider 320.

Hereinafter, the operation of the APC circuit shown in FIG. 5 will now be described in greater detail according to the APC modes.

1) Sub-APC mode

The APC circuit of FIG. 5 performs APC operations over a period of one sector in the sub-APC mode, and maintains the control value latched at the current mirror or gap area up to the following mirror or gap area. The latching at the mirror or gap area can be performed at any point throughout the entire area, and preferably, at the end point of the area.

The sub-APC mode is set by the control of the microcomputer. The control signal generator 310 generates a control signal, under the control of the microcomputer, which controls the APC controller 300 such that it operates in the sub-APC mode. Also, the control signal can control the APC controller 300 such that it operates while the mirror or gap signal MIRROR/GAP, or the division signal DV is applied.

The APC controller 300 latches a signal from the up/down counter 208, or the MUX 212, while it is enabled by the mirror or gap signal MIRROR/GAP, or the division signal DV. In the present embodiment, the APC controller 300 can latch and process 8 samples in the mirror or gap area. The control value latched by the APC controller 300 is applied through

the DAC 210 and the BUF 214 to the LD driver 140.

In the sub-APC mode, the APC controller 300 performs latching in a period of the mirror or gap signal MIRROR/GAP or of the division signal DV, so that the latched control value can be maintained until the following mirror or gap signal MIRROR/GAP, or division signal DV is applied. Thus, the power of the LD 160 can be maintained until the following mirror or gap signal MIRROR/GAP or division signal DV is applied.

2) Average APC mode

In the average APC mode, the APC circuit of FIG. 5 controls the LD driver 140 with the average of control values for a predetermined period. The average APC mode is set by the control of the microcomputer. The control signal generator 310 generates a control signal under the control of the microcomputer, which controls the APC controller 300 such that it operates in the average APC mode.

The APC controller 300 samples control values from the up/down counter 208 or the MUX 212, and calculates the average of a predetermined number of the sampled values. The up/down counters 208a through 208e and the multiplexers 212a and 212b are selected according to the operation mode. Thus, in a certain mode, one of the up/down counters 208a through 208e is selected and one of the multiplexers 212a and 212b is selected (if up/down counter 208a is not selected). The average is applied to the LD driver 140 through the DAC 210 and the BUF 214. In the average APC mode, the APC controller 300 controls the power of the LD 160 with the average of control values output for a predetermined period. The average APC mode provides an effect of low-pass-filtering control values, so that the APC operation in the average APC mode is resilient against external noise, which may contain an RF component.

3) Sub-average APC mode

In the sub-average APC mode, the APC circuit of FIG. 5 performs APC operation in a period of one sector, and maintains the average of the control values generated during the mirror or gap area up to the following mirror or gap area. The sub-average APC is set by the

control of the microcomputer. The control signal generator 310 generates a control signal under the control of the microcomputer, which controls the APC controller 300 such that it operates in the sub-average APC mode.

The APC controller 300 calculates the average of the control values from the up/down counter 208 or the MUX 212, while it is enabled by the mirror or gap signal MIRROR/GAP, or the division signal DV, and latches the calculated average. The up/down counters 208a through 208e and the multiplexers 212a and 212b are selected according to the operation mode. Thus, in a certain mode, one of the up/down counters 208a through 208e is selected and one of the multiplexers 212a and 212b is selected (if up/down counter 208a is not selected). In the present embodiment, 8 samples at the mirror or gap area are latched and processed. The average latched by the APC controller 300 is applied to the LD driver 140 through the DAC 210 and the BUF 214.

In the sub-average APC mode, the APC controller 300 latches the average of the control values in a period of the mirror or gap signal MIRROR/GAP, or of the division signal DV, so that the latched average of control values is maintained until the following mirror or gap signal MIRROR/GAP, or division signal DV is applied. In addition, controlling the power of the LD 160 with the average of control values generated during when the mirror or gap signal MIRROR/GAP, or division signal DV is applied, provides an effect of performing low-pass-filtering, the APC operation in the sub-average APC mode is resilient against external noise which may include an RF component.

4) Read mode

In the read mode, APC operation is performed by a loop which includes the latch 216, the fourth DAC 218, the fourth buffer 220, the first COMP 206a, the first up/down counter 208a, the APC controller 300, the first DAC 210a, the first BUF 214a, the LD driver 140, the LD 160, the PD 202 and the VGA 204. When the microcomputer is initialized, a desired power level for the LD 160 is simultaneously stored in the latch 216 for the read mode. The operation of the LD 160 is started by the power level stored in the latch 216.

The fourth DAC 218 converts the latched data from the latch 216 into analog data, and

the fourth BUF 220 outputs the analog data from the fourth DAC 218, as the first reference voltage Vref1 for the read mode, to the first COMP 206a. The first up/down counter 208a counts the decision signal from the first COMP 206a, the first DAC 210a converts the count value from the first up/down counter 208a into an analog value, and the first BUF 214a buffers the output from the first DAC 210a, and provides the result to the LD driver 140.

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The LD 160 outputs the power under the control of the LD driver 140, and the PD 202 detects the power level. The detected power level is provided as one input of the first COMP 206a through the VGA 204. If the power level from the LD 160 is higher than the power level which is latched by the latch 216, the decision signal from the first COMP 206a is asserted to a logic low, so that the first up/down counter 208a downcounts the decision signal by one. Accordingly, a lower control value is applied to the LD driver 140, and thus the power level from the LD 160 is decreased. Meanwhile, if the power from the LD 160 is lower than the power level which is latched by the latch 216, the decision signal from the first COMP 206a is asserted to a logic high, so that the first up/down counter 208a upcounts the decision signal by one. Accordingly, a higher control value is applied to the LD driver 140, thereby raising the power level from the LD 160.

The above operation is continued until the power level from the LD 160 reaches the power level latched by the latch 216.

5) Erase mode

In the erase mode, APC operation is performed by a loop which includes the latch 217, the third MUX 222, the fifth DAC 219, the fifth buffer 221, the second COMP 206b, the second and third up/down counters 208b and 208c, the first MUX 212a, the APC controller 300, the second DAC 210b, the second BUF 214b, the LD driver 140, the LD 160, the PD 202 and the VGA 204. When the microcomputer is initialized, a desired power level for the LD 160 is simultaneously stored in the latch 217 for the erase and record modes. The operation of the LD 160 is started by the power level stored in the latch 217.

In the erase mode, the optical output of a disc such as a DVD-RAM must be varied according to the type of tracks (lands or grooves), and thus the first latch 217a for lands and

the second latch 217b for grooves are used. The third MUX 222 selects the output of the first latch 217a or the second latch 217b according to the type of tracks. In particular, a signal for identifying lands or grooves, which is generated in a tracking servo control circuit, is used.

The fifth DAC 219 converts the data from the third MUX 222 into analog data, and the fifth BUF 221 outputs the analog data from the fifth DAC 219, as the second reference voltage Vref2 for the erase mode, to the second COMP 206b. The up/down counter 208 counts the decision signal from the second COMP 206b. In particular, the second up/down counter 208b for lands and the third up/down counter 208c for grooves, are used according to whether the track is a land or groove. The first MUX 212a selects the output of the second up/down counter 208b or the third down/up counter 208c, according to the type of tracks.

The second DAC 210b converts the count value from the second or third up/down counter 208b or 208c into an analog value, and the second BUF 214b buffers the analog value from the second DAC 210b, and provides the result to the LD driver 140. The LD 160 outputs the power under the control of the LD driver 140, and the PD 202 detects the power level. The detected power level is provided as one input of the second COMP 206b through the VGA 204.

6) Record mode

In the record mode, APC operation is performed by a loop which includes the latch 217, the third MUX 222, the fifth DAC 219, the fifth buffer 221, the second COMP 206b, the fourth and fifth up/down counters 208d and 208e, the second MUX 212b, the APC controller 300, the third DAC 210c, the third BUF 214c, the LD driver 140, the LD 160, the PD 202 and the VGA 204. When the microcomputer is initialized, a desired power level for the LD 160 is simultaneously stored in the latch 217 for the erase and record modes. The operation of the LD 160 is started by the power level stored in the latch 217.

In the record mode, the optical output of a disc such as a DVD-RAM must be varied according to the type of tracks (lands or grooves), and thus the third latch 217c for lands and the fourth latch 217b for grooves are used. The third MUX 222 selects the output of the third latch 217c or the fourth latch 217b according to the type of tracks.

The fifth DAC 219 converts the data from the third MUX 222 into analog data, and the fifth BUF 221 outputs the analog data from the fifth DAC 219, as the second reference voltage Vref2 for the record mode, to the second COMP 206b. The up/down counter 208 counts the decision signal from the second COMP 206b. In particular, the fourth up/down counter 208d for lands and the fifth up/down counter 208e for grooves, are used according to whether the track is a land or groove. The second MUX 212b selects the output of the fourth up/down counter 208d or the fifth down/up counter 208e, according to the type of tracks.

The third DAC 210c converts the count value from the fourth or fifth up/down counter 208d or 208e into an analog value, and the third BUF 214c buffers the analog value from the third DAC 210c, and provides the result to the LD driver 140. The LD 160 outputs the power under the control of the LD driver 140, and the PD 202 detects the power level. The detected power level is provided as one input of the second COMP 206b through the VGA 204.

In the present embodiment, the APC circuit according to the present invention periodically operates according to the three sub-divided APC modes, that is, according to the sub-APC mode, the average APC mode and the sub-average APC mode. However, the APC circuit can also operate continuously through the entire APC mode, as does the conventional APC circuit shown in FIG. 1.

As described above, the APC circuit according to the present invention periodically controls the power level of the LD, unlike the conventional APC circuit having the continuous operating characteristic, so that the laser power level may remain constant, and resilience to external noise can also be obtained. Also, the APC operation is performed at a non-effective data area, not at the effective data area, so that accurate recording/playback result can be ensured.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.